GENERAL DESCRIPTION

TRS4BMXXF series are 4bit micro-controller which could play 4 channel melody or 4 channel ADPCM with PWM direct drive circuit. PWM resolution is 10 bits. TRS4BMXXF series includes a low cost, high performance CMOS micro-processor. The clock frequency of this up is typically 8.1 (±5%) MHz. This chip operates over a wide voltage range of 2.4V~5.5V. It contains program ROM and data ROM inside. The maximum program ROM is 16K and maximum data ROM size is 20K~512K byte. The maximum working SRAM is (128+2) nibbles. It is provided with total 16 I/O Ports, including 12 software programmable I/O Ports, and 4 fixed output ports .

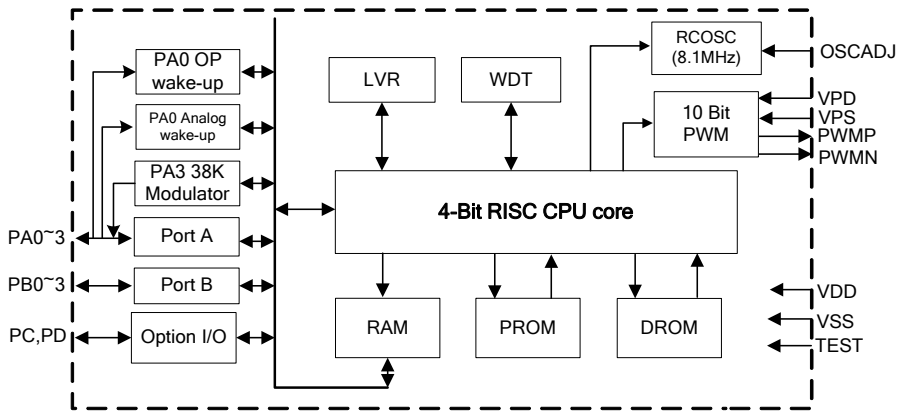
FEATURES

- Low cost and high performance microprocessor.
- Wide operating voltage 2.4V~5.5V.
- 16K word program ROM.
- 20K~512K byte data ROM.
- (128+2) nibbles SRAM.
- 12 software programmable I/O ports, 4 fixed output ports.
- Mask option for I/O port wake up function.
- Mask option for 50k/1M pull-down resistor.
- Mask option for RESETB pin select.
- Mask option for low voltage reset.
- Standby mode for power saving.
- One PWM audio output.
- Wavetable function.
- PA0 is provided with a low power analog input (Schmitt) for wake-up control (Mask option).
- PA3 built-in 38KHz modulator (Mask option)
- Support level shifter for VPD and VDD two power supply application. (**VPD=5V, VDD=2.4V~5V, VPD>=VDD, VDD > VPD not allowed**)
- PA,PB,PC,PD are provided with high sink current 20mA @VDD=3V (V_{OL}=1V)
- PB0~PB3 are provided with high driving current 10mA @VDD=3V, V_{OH}=2V (HDEN Mask option), **TRS4BM95F** , **TRS4BM128F** and **TRS4BM170F** series are not provided this function.
- PA0 is provided with a low power analog input (OP Amplifier) for wake-up control (BZWK Mask option). Only **TRS4BM32F** and **TRS4BM42F** series are provided this function.

The RAM ROM sizes and I/O ports of TRS4BMXXF are shown below：

BODY	TRS4BM06F	TRS4BM10F	TRS4BM16F	TRS4BM21F	TRS4BM32F	TRS4BM42F
VOICE DURATION	6 SEC.	10 SEC.	16 SEC.	21 SEC.	32 SEC.	42 SEC.
RAM SIZE	(96+2) x 4	(96+2) x 4	(96+2) x 4	(96+2) x 4	(96+2) x 4	(96+2) x 4
I/O PINS	12I/O , 4O	12I/O , 4O	12I/O , 4O	12I/O , 4O	12I/O , 4O	12I/O , 4O
DATA ROM SIZE	20K x 8	32K x 8	48K x 8	64K x 8	96K x 8	128K x 8
PROGRAM ROM SIZE	8K x 12	8K x 12	8K x 12	8K x 12	8K x 12	8K x 12
BODY	**TRS4BM52F**	**TRS4BM64F**	**TRS4BM95F**	**TRS4BM128F**	**TRS4BM170F**	**---**
VOICE DURATION	52 SEC.	64 SEC.	95 SEC.	128 SEC.	170 SEC.	---
RAM SIZE	(96+2) x 4	(96+2) x 4	(128+2) x 4	(128+2) x 4	(128+2) x 4	---
I/O PINS	12I/O , 4O	12I/O , 4O	12I/O , 4O	12I/O , 4O	12I/O , 4O	---
DATA ROM SIZE	156K x 8	192K x 8	285K x 8	384K x 8	512K x 8	---
PROGRAM ROM SIZE	8K x 12	8K x 12	16K x 12	16K x 12	16K x 12	---

BLOCK DIAGRAM



PIN DESCIRPTION

PAD Name	Type	State After Reset	Description
Power Input			
VDD	P	High	Power input except PWM block power
VSS	P	Low	Ground input except PWM block power
VPD	P	High	PWM block power input, **Support VPD and VDD two power supply application, (VPD=5V, VDD=2.4~5V, VPD>=VDD, VDD > VPD not allowed)**
VPS	P	Low	PWM block ground input
General I/O ports			
PA0~PA3	I/O	XXXX	Port A is a programmable Input /Output port. PA0 shared with analog or OP Amp. input port for wake-up by mask option. PA3 built-in a 38KHz modulator by mask option.
PB0~PB2	I/O	XXXX	PB0~PB2 is a programmable Input /Output pin, high drive current 10mA is enabled by mask option.
PB3/RESETB	I/O(I)	X/H	PB3 shared with RESETB by mask option, PB3 high drive current 10mA is enabled by mask option.
PC0~PC2	O	000/XXX	PC0~PC2 is a output port only.
PC3/RESETB	O/I	0/H	PC3 is a output port only ,it shared with RESETB by mask option.
PD0~PD3	I/O	XXXX	Port D is a programmable Input /Output port.
TEST PIN			
TEST	I	Low	For testing use, it is pull down to VSS internal chip.
Audio output pin			
PWMP	I/O	Low	Audio output PWM (+).
PWMN	I/O	Low	Audio output PWM (-).
OSC PIN			
OSCADJ	I	X	Frequency adjust pin, connected to external resistor to VSS for adjusting oscillator frequency.

Note : Substrate must be connected to VSS.

FUNCTION DESCRIPTION

DATA DROM (DROM)

The TRS4BMXXF series are provided with 20K~512K bytes ROM for data storage. DROM is addressed by five registers DMA4, DMA3, DMA2, DMA1 and DMA0, where DMA0 is the lowest nibble while DMA4 is the highest one. After these registers are specified by software, data is read from data register (DMDL & DMDH) and it need enough delay time (**about 5 MCU instruction time**) for access time requirement, where DMDL is the low nibble while DMDH is high nibble.

PROGRAM ROM (PROM)

The TRS4BMXXF series are provided with 8K~16K words (0000H ~ 3FFFH) PROM which stores execution program.

SRAM

The TRS4BMXXF series are provided with 96~128 nibbles SRAM. The addressing space is separated into several pages. Program can select working pages by setting MAH register.

HALT MODE

The TRS4BMXXF series are provided with a power saving mode for those applications requiring a very low stand-by current. The PA0~PA3, PB0~PB3, PD0~PD3 are the wake-up sources. Furthermore, the SRAM will keep their previous setting without any data loss in this mode. Low voltage reset (LVR) will be disabled in halt mode automatically for saving power consumption.

I/O PORT

TRS4BMXXF series are provided with four sets I/O ports. PA0~PA3, PB0~PB3 and PD0~PD3 are input/output programmable, PC0~PC3 is output port only. All three ports PA, PB, PD are in input port mode after reset, and if wake-up option is enabled, they will be turned to input port mode automatically after MCU execution HALT instruction. When PA,PB,PD bit set to be wake-up enabled and MCU is in halt mode, a rising edge at that pin will wake up MCU after 64 MCU cycles, and then MCU will jump to address 004H. All output port PA0~PA3, PB0~PB3, PC0~3 and PD0~PD3 are provided with high sink 20mA current.

Several hardware options are provided for I/O ports. They are described as the followings:

- PA0~PA3, PB0~PB3, PD0~PD3, could be selected to have wake-up function or not.
- PA0~PA3, PB0~PB3, PD0~PD3, could be selected to have 50K/1M ohm pull down resistor or not when in input mode.
- PB3 and PC3 could be selected as RESETB pin or not.
- PC0~PC3 and PD0~PD3 could be selected to have output low open or not.
- PC0~PC3 and PD0~PD3 could be selected to have output high when in power down mode (halt).

PA0 is provided with an analog input (Schmitt) for wake-up control (Mask option)

PA0 supports an analog input buffer with schmitt circuit, it is enabled by **"RCWK" option** and supports low power consumption in halt mode, if PA0 analog signal keep about 0.5VDD, so this function is suitable for recycle wakeup MCU by external RC time constant, external RC time constant is easy built by VDD connected to R and serial with C to VSS.

PA0 is provided with an analog input (OP Amp.) for wake-up control (Mask option)

It built-in an OP amplifier for wakeup trigger, the pull down 1M and 50k resistor will be disabled by hardware circuit when "**BZWK" option is** enabled automatically, PA0 always keep at DC level (bias voltage Vbias) for signal amplify, and Vbias is about 0.8V ~ 1.0V. Only **TRS4BM32F** and **TRS4BM42F** series are provided this function.

PA3 is provided with a 38KHz modulator (Mask option)

PA3 built-in a 38KHz modulator combined with register DATA_PA bit 3, this function is enabled by "**F38K" option.**

PB0~PB3 is provided with high driving current 10mA (HDEN Mask option)

The driving current of Port B is about 3.5mA normally, it can support 10mA driving current if needed by mask option.

TRS4BM95F , **TRS4BM128F** and **TRS4BM170F** series are not provided this function.

10bit PWM AUDIO OUTPUT

TRS4BMXXF series have one set of PWM for audio output. The PWM output can drive 8 ohm speaker. It can be enabled or disabled by software programming. The PWM is 10 bit resolution. And its clock is set as 32KHz. The PWM data registers are

AUD_DL and AUD_DH, where AUD_DL is the low nibble and AUD_DH is the high nibble.

LOW VOLTAGE RESET (LVR)

The TRS4BMXXF series could be selected to have low voltage reset function or not. If this option is enabled, the system will reset automatically when supply voltage is too low, it will be disabled in halt mode.

WATCH DOG TIMER (WDT)

There is a watch dog timer available in this chip. This timer can be enabled or disabled by hardware option. When disabled, watch dog timer will not have any effect to chip. When enabled, software shall run an "reset watch dog" instruction before this timer time out.

SYSTEM RESET

The system reset signal is combine with four signals which are power on reset, low voltage reset (LVR), external PC3/PB3 (RESETPIN) pin and WDT overflow reset.

RC OSCILLATOR

The chip has an standard frequency of 8.1 MHz, built from RC oscillator. The frequency can be adjusted by using external resistor connected between OSCADJ pin and VSS, the resistor is from 0 to 100K ohm for ±10% deviation. When external resistor is used, internal resistor is abandoned. All chips of the series has accurate clock generator, it may be in range ±5 % of mass production. System clock can be stopped by HALT command. Once stopped, only wake-up triggering inputs or PB3/PC3 (RESETB) input (if option is enabled) can re-start oscillation.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYSMBOL	RATING	UNIT
DC Supply Voltage	V+	< 7.0	V
Input Voltage Range	V_{IN}	-0.5 to VDD+0.5	V
Operating Temperature	T_A	-10 to 60	ºC
Storage Temperature	T_{STO}	-50 to 150	ºC

DC CHARACTERISTICS (TA = 25℃, VDD = 3V, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
Operating voltage	V_{DD}	-	2.4	-	5.5	V
Operating Current	I_{OP}	3V , 8.1MHz	-	2.5	-	mA
Standby Current (RCWK & BZWK option disabled)	I_{STBY_A}	1.VDD=5V 2.PA0 RCWK option disabled 3.PA0 BZWK option disabled	-	0.1	1	uA

Standby Current (RCWK option enabled)	I_{STBY_B1}	1.VDD=5V, PA0=2.5V 2.PA0 RCWK option enabled 3.PA0 BZWK option disabled	-	4	6	uA
Standby Current (BZWK option enabled)	I_{STBY3_C1}	1.VDD=5V 2.PA0 BZWK option enabled 3.PA0 RCWK option disabled	-	30		uA
Input High Level	V_{IH}	All I/O port	$0.8*V_{DD}$	-	-	V
Input Low Level	V_{IL}	All I/O port	-	-	$0.2*V_{DD}$	V
Input High Level	V_{IH_PA0}	RCWK option enabled	$0.74*V_{DD}$	-	-	V
Input Low Level	V_{IL_PA0}	RCWK option enabled	-	-	$0.34*V_{DD}$	V
Output Drive Current	I_{OH1}	VDD=3V , V_{OH}=2V	-	-3.5	-	mA
Output High Drive Current	I_{OH2}	VDD=3V , V_{OH}=2V (For PB0~3, HDEN option=1)	-	-10	-	mA
Output High Sink Current	I_{OL1}	VDD=3V , V_{OL}=1V (For PA,PB,PC,PD)	-	20	-	mA
Input Resistor	R_{IN}	Pull down 50K ohm Selected VDD=4.5V	-	50	-	Kohm
		Pull down 1M ohm Selected	-	1000	-	Kohm

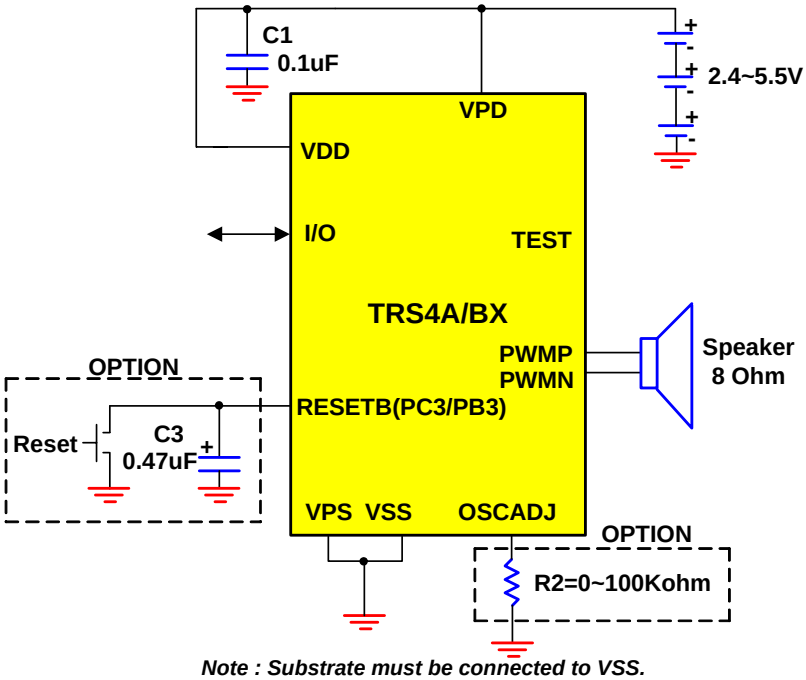
AC CHARACTERISTICS (TA = 25℃, VDD = 3V, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMIT			UNIT
			Min	Typ	Max	
RCOSC Frequency	F_{CPU1}	OSCADJ PAD floating VDD=2.4V~5.5V	7.7	8.1 (8.1±5%)	8.5	MHz
	F_{CPU2}	OSCADJ PAD connected with 0~100K ohm resistor to VSS		8.1±10%		MHz
PA3 38KHz output	F_{38K}	PA3 F38K option enabled and register DATA_PA=1xxx B	-	F_{CPU1}÷216		KHz
DROM data ready time	Tdrom	Address ready to data ready			5 instruction cycles	
Stable clock delay after RCOSC clock output	CKstable2	CKstable (Note1)	-	64		MCU cycle (1/8M)

Note1: The stable clock delay is place after first clock output of RCOSC and before user's first instruction, it means the user's program will get more stable clock after power on reset or wakeup from halt mode.

APPLICATION CIRCUIT

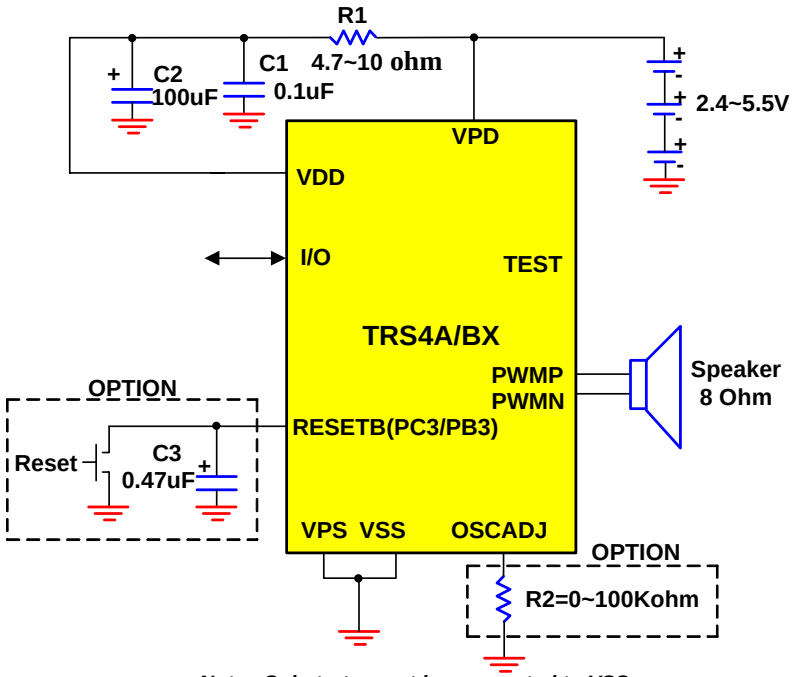
(1) Normal circuit



Note : Substrate must be connected to VSS.

(2) Heavy loading circuit

This application circuit is used when internal impendence of battery is high and/or speaker volume is high and/or heavy load is used at PWMP or PWMN PIN (like Motor).



Note : Substrate must be connected to VSS.

REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
V1.0	New		2009.07.14
V1.1	PA3 provide 38KHz modulator	P3,P5	2009.09.24
V1.2	1. Modify AC/DC characteristics 2. RC Oscillator frequency 8.1±5% MHz	P1,P6,P12,P13	2010.01.06
V1.3	1. Only **TRS4BM32F** and **TRS4BM42F** series are provided option "BZWK" 2. About 5 MCU instruction time 3. DC characteristics	P1, P4 P3 P5,P6	2010.08.12
V1.4	1. **TRS4BM95F** , **TRS4BM128F** and **TRS4BM170F** series are not provided this function.	P1	2010.03.04
V1.5	1. Output sink current 5mA	P6	2013.04.12